Practitioner's Docket No. 56426

CHAPTER II

TRANSMITTAL LETTER
TO THE UNITED STATES ELECTED OFFICE (EO/US)
(ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)

PCT/DE00/00681	03 March 2000	04 March 1999
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED

METHOD AND CIRCUIT ARRANGEMENT FOR PICTURE-IN-PICTURE INSERTION
TITLE OF INVENTION

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APPLICANTS

Box PCT
Assistant Commissioner for Patents
Washington D.C. 20231
ATTENTION: EO/US

NOTE: To avoid abandonment of the application, the applicant shall furnish to the USPTO, not later than 20 months from the priority date: (1) a copy of the international application, unless it has been previously communicated by the International Bureau or unless it was originally filed in the USPTO, and (2) the basic national fee (see 37 C.F.R. § 1.492(a)). The 30-month time limit may not be extended. 37 C.F.R. § 1.495.

WARNING: *Where the items are those which can be submitted to complete the entry of the international application into the national phase are subsequent to 30 months from the priority date the application is still considered to be in the international state and if mailing procedures are utilized to obtain a date the express mail procedure of 37 C.F.R. §1.10 must be used (since international application papers are not covered by an ordinary certificate of mailing - See 37 C.F.R. §1.8.*

NOTE: Documents and fees must be clearly identified as a submission to enter the national state under 35 USC 371 otherwise the submission will be considered as being made under 35 USC 111. 37 C.F.R. § 1.494(f).

CERTIFICATION UNDER 37 C.F.R. § 1.10*
*(Express Mail label number is **mandatory**.)*
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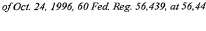
I hereby certify that this paper, along with any document referred to, is being deposited with the United States Postal Service on this date August 31, 2001, in an envelope as "Express Mail Post Office to Addressee," mailing Label Number **EK835032915US**, addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231.

Deanna M. Rivernider
(type or print name of person mailing paper)



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1. Applicant herewith submits to the United States Elected Office (EO/US) the following items under 35 U.S.C. 371:

   a. [X] This express request to immediately begin national examination procedures (35 U.S.C. 371(f)).

   b. [X] The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees (37 C.F.R. § 1.492) as indicated below:

2. Fees

CLAIMS FEE [X]*	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	10- 20 =	0	x $ 18.00 =	$0
	INDEPENDENT CLAIMS	2 - 3 =	0	x $ 80.00 =	$0
	MULTIPLE DEPENDENT CLAIM(S) (if applicable) + $270.00				$
BASIC FEE**	[ ] U.S. PTO WAS INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where an International preliminary examination fee as set forth in § 1.482 has been paid on the international application to the U.S. PTO: [ ] and the international preliminary examination report states that the criteria of novelty, inventive step (non-obviousness) and industrial activity, as defined in PCT Article 33(2) to (4) have been satisfied for all the claims presented in the application entering the national stage (37 CFR 1.492(a)(4)) ..... $96.00 [ ] and the above requirements are not met (37 CFR 1.492(a)(1)) ..... $670.00 [X] U.S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in § 1.482 has been paid to the USPTO, and payment of an international search fee as set forth in § 1.445(a)(2) to the U.S. PTO: [ ] has been paid (37 CFR 1.492(a)(2)) ..... $760.00 [ ] has not been paid (37 CFR 1.492(a)(3)) ..... $970.00 [X] where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 CFR 1.492(a)(5)) $860.00				$860.00
				Total of above Calculations	= $860.00
SMALL ENTITY	Reduction by ½ for filing by small entity, if applicable. Affidavit must be filed. (note 37 CFR 1.9, 1.27, 1.28)				- $
				Subtotal	$860.00
				Total National Fee	$860.00
	Fee for recording the enclosed assignment document $40.00 (37 CFR 1.21(h)). (See Item 13 below). See attached "ASSIGNMENT COVER SHEET".				$
TOTAL				Total Fees enclosed	$860.00

*See attached Preliminary Amendment Reducing the Number of Claims.

i. [X] A check in the amount of $860.00 to cover the above fees is enclosed.

ii. [ ] Please charge Account No. _____ in the amount of $ _____.

A duplicate copy of this sheet is enclosed.

***WARNING:* *"To avoid abandonment of the application the applicant shall furnish to the United States Patent and Trademark Office not later than the expiration of 30 months from the priority date: * * * (2) the basic national fee (see § 1.492(a)). The 30-month time limit may not be extended." 37 C.F.R. § 1.495(b).*

WARNING: *If the translation of the international application and/or the oath or declaration have not been submitted by the applicant within thirty (30) months from the priority date, such requirements may be met within a time period set by the Office. 37 C.F.R. § 1.495(b)(2). The payment of the surcharge set forth in § 1.492(e) is required as a condition for accepting the oath or declaration later than thirty (30) months after the priority date. The payment of the processing fee set forth in § 1.492(f) is required for acceptance of an English translation later than thirty (30) months after the priority date. Failure to comply with these requirements will result in abandonment of the application. The provisions of § 1.136 apply to the period which is set. Notice of Jan. 3, 1993, 1147 O.G. 29 to 40.*

3. [X] A copy of the International application as filed (35 U.S.C. 371(c)(2)):

NOTE: *Section 1.495 (b) was amended to require that the basic national fee and a copy of the international application must be filed with the Office by 30 months from the priority date to avoid abandonment "The International Bureau normally provides the copy of the international application to the Office in accordance with PCT Article 20. At the same time, the International Bureau notifies applicant of the communication to the Office. In accordance with PCT Rule 47.1, that notice shall be accepted by all designated offices as conclusive evidence that the communication has duly taken place. Thus, if the applicant desires to enter the national stage, the applicant normally need only check to be sure the notice from the International Bureau has been received and then pay the basic national fee by 30 months from the priority date." Notice of Jan. 7, 1993, 1147 O.G. 29 to 40, at 35-36. See item 14c below.*

a. [ ] is transmitted herewith.
b. [ ] is not required, as the application was filed with the United States Receiving Office.
c. [X] has been transmitted
   i. [X] by the International Bureau.
   Date of mailing of the application (from form PCT/IB/308): _____.
   ii. [ ] by applicant on _____.
   Date

4. [X] A translation of the International application into the English language (35 U.S.C. 371(c)(2)):
a. [X] is transmitted herewith.
b. [ ] is not required as the application was filed in English.
c. [ ] was previously transmitted by applicant on _____.
   Date
d. [ ] will follow.

5. [X] Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. 371(c)(3)):

NOTE: *The Notice of January 7, 1993 points out that 37 C.F.R. § 1.495(a) was amended to clarify the existing and continuing practice that PCT Article 19 amendments must be submitted by 30 months from the priority date and this deadline may not be extended. The Notice further advises that: "The failure to do so will not result in loss of the subject matter of the PCT Article 19 amendments. Applicant may submit that subject matter in a preliminary amendment filed under section 1.121. In many cases, filing an amendment under section 1.121 is preferable since grammatical or idiomatic errors may be corrected." 1147 O.G. 29-40, at 36.*

a. [ ] are transmitted herewith.
b. [ ] have been transmitted
   i. [ ] by the International Bureau.

Date of mailing of the amendment (from form PCT/IB/308): _____.

ii. [ ] by applicant on _____.
Date

c. [X] have not been transmitted as

i. [X] applicant chose not to make amendments under PCT Article 19.
Date of mailing of Search Report (from form PCT/ISA/210): **18/08/2000**

ii. [ ] the time limit for the submission of amendments has not yet expired. The amendments or a statement that amendments have not been made will be transmitted before the expiration of the time limit under PCT Rule 46.1.

6. [X] A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. 371(c)(3)):

a. [ ] is transmitted herewith.
b. [ ] is not required as the amendments were made in the English language.
c. [X] has not been transmitted for reasons indicated at point 5(c) above.

7. [X] A copy of the international examination report (PCT/IPEA/409)

[X] is transmitted herewith.
[ ] is not required as the application was filed with the United States Receiving Office.

8. [ ] Annex(es) to the international preliminary examination report

a. [ ] is/are transmitted herewith.
b. [ ] is/are not required as the application was filed with the United States Receiving Office.

9. [ ] A translation of the annexes to the international preliminary examination report

a. [ ] is transmitted herewith.
b. [ ] is not required as the annexes are in the English language.

10. [X] An oath or declaration of the inventor (35 U.S.C. 371(c)(4)) complying with 35 U.S.C. 115

a. [ ] was previously submitted by applicant on _____.
Date

b. [ ] is submitted herewith, and such oath or declaration

i. [ ] is attached to the application.
ii. [ ] identifies the application and any amendments under PCT Article 19 that were transmitted as stated in points 3(b) or 3(c) and 5(b); and states that they were reviewed by the inventor as required by 37 C.F.R. 1.70.
iii. [X] will follow.

II. Other document(s) or information included:

11. [X] An International Search Report (PCT/ISA/210) or Declaration under PCT Article 17(2)(a):

a. [X] is transmitted herewith.
b. [ ] has been transmitted by the International Bureau.
Date of mailing (from form PCT/IB/308): _____.
c. [ ] is not required, as the application was searched by the United States International Searching Authority.

d. [ ] will be transmitted promptly upon request.
e. [ ] has been submitted by applicant on _____.
Date

12. [X] An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98:
a. [X] is transmitted herewith.
Also transmitted herewith is/are:
[X] Form PTO-1449 (PTO/SB/08A and 08B).
[X] Copies of citations listed.
b. [ ] will be transmitted within THREE MONTHS of the date of submission of requirements under 35 U.S.C. 371(c).
c. [ ] was previously submitted by applicant on _____.
Date

13. [ ] An assignment document is transmitted herewith for recording.

A separate [ ] "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or [ ] FORM PTO 1595 is also attached.

14. [X] Additional documents:
a. [X] Copy of request (PCT/RO/101)
b. [X] International Publication No. WO 00/52931
i. [X] Specification, claims and drawing
ii. [ ] Front page only
c. [ ] Preliminary amendment (37 C.F.R. § 1.121)
d. [X] Other

Preliminary Amendment, Forms PCT/IB/304, PCT/IB/306, International Preliminary Examination Report, English translation of the amended pages filed under Art. 34 PCT (Annex to the International Preliminary Examination Report).

15. [X] The above checked items are being transmitted
a. [X] before 30 months from any claimed priority date.
b. [ ] after 30 months.

16. [ ] Certain requirements under 35 U.S.C. 371 were previously submitted by the applicant on _____, namely:

AUTHORIZATION TO CHARGE ADDITIONAL FEES

WARNING: *Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges if extra claims are authorized.*

NOTE: "A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).

NOTE: "Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).

[X] The Commissioner is hereby authorized to charge the following additional fees that may be required by this paper and during the entire pendency of this application to Account No. **04-1105.**

[X] 37 C.F.R. 1.492(a)(1), (2), (3), and (4) (filing fees)

WARNING: *Because failure to pay the national fee within 30 months without extension (37 C.F.R. § 1.495(b)(2)) results in abandonment of the application, it would be best to always check the above box.*

[X] 37 C.F.R. 1.492(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1.492(d)), it might be best not to authorize the PTO to charge additional claim fees, except possible when dealing with amendments after final action.

[X] 37 C.F.R. 1.17 (application processing fees)
[X] 37 C.F.R. 1.17(a)(1)-(5)(extension fees pursuant to § 1.136(a).
[ ] 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 C.F.R. § 1.311(b).

NOTE: 37 C.F.R. 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying . . . issue fee." From the wording of 37 C.F.R. § 1.28(b): (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

[ ] 37 C.F.R. § 1.492(e) and (f) (surcharge fees for filing the declaration and/or filing an English translation of an International Application later than 30 months after the priority date).

/SIGNATURE OF PRACTITIONER

Reg. No.: 33,860 — Peter F. Corless
(type or print name of practitioner)

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Docket No. 56426

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: M. Brett et al.

EXPRESS MAIL LABEL: EL 835032915US

FILED: HEREWITH

FOR: METHOD AND CIRCUIT FOR PICTURE-IN-PICTURE SUPERIMPOSITION

THE HONORABLE COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231

SIR:

PRELIMINARY AMENDMENT

Applicants file herewith the above-identified application. Please amend the application as follows.

IN THE CLAIMS

Please cancel claims 1-10 without prejudice.

Please add the following new claims.

11. A method for picture-in-picture insertion, in which a sequence of decimated inset pictures is written to a memory device and is read out for insertion into a sequence of main pictures,

wherein inset pictures are written to the memory device in a circulating manner as fields under continuously incremented write addresses, the inset pictures being written to corresponding memory segments beginning at corresponding writing start addresses, in that the writing start address of each written-in field is stored,

in that, each time the write address is incremented, by comparison of the respective instantaneous write address with a previously stored writing start address, an overtake signal is formed which indicates whether the respective writing start address is reached again and the

memory segment corresponding to the respective writing start address is overwritten, in that, by evaluation of the overtake signal, the memory segment corresponding to the last writing start address stored or the penultimate writing start address stored is selected for read-out, and

in that the selected memory segment is read out for insertion into the respective main picture with continuously incremented read addresses.

12. The method of claim 11 wherein the write and read addresses are continuously incremented from a first memory address up to a last memory address and are in each case reset to the first memory address again after the last memory address has been reached.

13. The method of claim 11 wherein in order to insert an inset picture into a main picture, in a segment buffer for two inset pictures, the picture position and size are in each case stored in the form of a number of lines and also pixels per line.

14. The method of claim 11 wherein the raster correction is effected by comparison between the raster position of a picture to be displayed and the raster position of a stored picture and also by skipping or repeating a line.

15. The method of claim 11 wherein each time the write address is incremented, the instantaneous write address is compared with the penultimate writing start address stored and, in the event of correspondence, the last writing start address stored is used as reading start address for reading the corresponding memory segment, whereas otherwise the penultimate writing start address is used as reading start address for reading the corresponding memory segment.

16. A circuit arrangement for inserting a sequence of decimated inset pictures into a sequence of main pictures, comprising:

a write controller for writing the inset pictures as fields under continuously incremented write addresses to corresponding memory segments of a memory device beginning at corresponding writing start addresses,

having a segment buffer for storing the writing start address of each field written to the memory device, in which case an overtake signal can be generated by the write controller each time the write address is incremented, by comparing the respective instantaneous write address with a previously stored writing start address, which overtake signal indicates whether the respective writing start address is reached again and the memory segment of the memory device which corresponds to the respective writing start address is overwritten,

having a display controller to which the overtake signal is fed, in which case the display controller can select, by evaluating the overtake signal, the memory segment corresponding to the last writing start address stored or the penultimate writing start address stored, for read-out by a read controller, connected to the segment buffer, with the aid of continuously incremented read addresses and for insertion into the respective main picture.

17. The circuit arrangement of claim 16 wherein the write controller and the read controller each have an address counter for incrementing the write addresses and read addresses, respectively.

18. The circuit arrangement of claim 16 wherein, by means of the display controller, an insertion position of an inset picture is calculated and a corresponding insertion signal can be fed to an insertion apparatus.

19. The circuit arrangement of claim 16 wherein, by means of the display controller, raster correction can be carried out by comparison between the raster position of a picture to be displayed and the raster position of a stored picture and also by skipping or repeating a line.

20. The circuit arrangement of claim 16 wherein provision is made of a comparator for comparing the instantaneous write address provided by an address counter with the penultimate writing start address stored, the output of the comparator being connected to a flip-slop for driving a multiplexer, and

in that the penultimate writing start address stored is present at a first input of the multiplexer and the last writing start address stored is present at a second input of the multiplexer, with the result that, in the event of correspondence between the instantaneous write address of the address counter and the penultimate writing start address stored, the multiplexer outputs the last writing start address stored as reading start address, whereas otherwise the multiplexer outputs the penultimate writing start address stored as reading start address.

REMARKS

To reduce initial filing fees, claims 1-10 have been cancelled without prejudice, and claims 11-20 have been added. No new matter has been added by virtue of the new claims. For instance, support for the new claims appears e.g. in the original claims of the application.

Early consideration and allowance of the application are earnestly solicited.

Respectfully submitted,

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5/PRTS

Description

Method and circuit arrangement for picture-in-picture insertion

The invention relates to a method for picture-in-picture insertion, in which a sequence of decimated inset pictures is written to a memory with at least two segments and is read out for insertion into a sequence of main pictures, to be precise in accordance with the preamble of claim 1, and also a circuit arrangement for picture-in-picture insertion, in particular for carrying out said method in accordance with the preamble of claim 6.

Various methods and apparatuses for inserting one or more inset pictures into a main picture (PIP - Picture In Picture) are known. In this case, the inset pictures stored in the memory are read out synchronously with a main picture. Since the read-out speed is generally higher, in a manner corresponding to the decimation of the inset picture, than the write-in speed, a seam can occur in the inset picture on account of the write pointer being overtaken by the read pointer, since the inset picture is then composed of a current part and a preceding part.

In particular in the case where the two parts originate from different motion phases, a disturbing effect is produced since moving objects through which the seam passes are displayed in a distorted manner. Moreover, if the frequencies of the inset and main pictures do not correspond exactly, the seam drifts, which is perceived as particularly unpleasant.

EP 0 739 130 A2 discloses, for the purpose of avoiding this problem, storing two inset pictures (or fields in each case) in the memory device, so that it is always the case that exactly one picture can be read out while

the next picture is written. Although this prevents the write pointer from being overtaken by the read pointer, there is nonetheless a significant disadvantage in that the storage capacity must be very high, which is associated with considerable costs.

The invention is based on the object, therefore, of providing a method and also a circuit arrangement for picture-in-picture insertion of the type mentioned in the introduction by means of which, with relatively low outlay, an inset picture can be generated without a seam.

This object is achieved by means of a method which is distinguished by the fact that:

- the inset pictures are written to the memory device in a circulating manner under continuously incremented write addresses,
- the first address of each written-in inset picture is stored,
- an overtake signal is formed by comparing the instantaneous address with a previously stored address, said signal indicating whether a previous address has been reached again and, consequently, the corresponding picture content has been overwritten,
- by evaluation of the overtake signal, the current or preceding segment is selected for read-out depending on whether or not overtaking took place before the start of the read-out, and
- the inset picture stored in the selected segment is read out with continuously incremented read addresses and is inserted into the main picture.

The object is furthermore achieved by means of a circuit arrangement for inserting a sequence of decimated inset pictures into a sequence of main pictures, which has a memory device having at least two segments for the inset pictures, a write controller and a read controller and which is distinguished in

particular by the fact that an overtake signal that can be fed into a display controller can be generated by the write controller, in that a segment buffer is provided, which segment buffer is connected to the read controller and serves to store a first and a last address of an inset picture, and in that a memory segment to be read out by the read controller can be selected by means of the display controller in a manner dependent on the overtake signal.

The solutions according to the invention are based on the insight that the write pointer can be prevented from being overtaken by the read pointer through suitable circulating addressing of the memory device in a manner utilizing the speed difference between the pointers. A significant advantage of this solution is that this holds true even when the size of the inset picture changes. Furthermore, is also not necessary to provide completely separate memory areas for reading and writing or to adapt the organization of the memory to the inset-picture size.

The subclaims contain advantageous developments of the invention.

Accordingly, for example, the write and read addresses are continuously incremented from a first memory address up to a last memory address and are in each case reset to the first memory address again after the last memory address has been reached.

For this purpose, in the circuit arrangement according to the invention, it is preferably provided that the write controller and the read controller each have an address counter for incrementing the write addresses and read addresses, respectively.

Further details, features and advantages of the invention emerge from the following description of

preferred embodiments with reference to the drawings, in which:

Figure 1 shows a block diagram of a circuit arrangement according to the invention;

Figure 2 shows a diagram of the signal profiles when writing to a picture memory;

Figure 3 shows a diagram of the signal profiles when reading from a picture memory;

Figure 4 shows a representation for illustrating the origination of a seam;

Figure 5 shows a diagram of the signal profiles according to the invention;

Figure 6 shows a block diagram of a circuit arrangement for selecting a memory segment;

Figure 7 shows an address pointer representation in the absence of vertical decimation;

Figure 8 shows a representation of memory division in the absence of vertical decimation, and

Figure 9 shows a representation of the memory outlay in the case of decimation.

In accordance with Figure 1, a main picture signal is fed to a circuit arrangement according to the invention via a first input A, and an inset picture signal is fed via a second input B. The inset picture signal passes to a decimation device 1 and also to a synchronization device 8. The picture signal of the inset picture, which is generally vertically decimated, is buffer-stored in the form of fields in a memory 2 and, after read-out, is fed together with the main picture signal

to an insertion apparatus 3, which generates a composite picture signal.

The synchronization device 8 is connected to the decimation device 1 via a first output and to a write controller 4 via a second output. A first output of the write controller 4 is connected to the memory 2, while a second output is connected to a segment buffer 7 and a third output is connected to a display controller 6. The output of the segment buffer 7 is connected to a read controller 5, to which a first output of the display controller 6 is also fed. An output of the read controller 5 is connected to the memory 2. Finally, a second output of the display controller is fed to the insertion apparatus 3, the display controller having an input C for synchronization signals of the main picture.

In order to write to the memory 2 an inset picture signal that has been decimated by the decimation device 1, the write controller 4 generates the required addresses. In the simplest case, given an e.g. linear organization of the memory 2, the write address pointer is incremented after each write operation. If the address pointer reaches the last address, it is reset to the first address, under which the writing process is continued, this being done over the duration of the field with interruptions in accordance with the decimation. In this case, a preceding picture (field) is inevitably overwritten.

With each beginning of a new field, the first write address is stored in the segment buffer 7, which additionally stores the last address as well. Furthermore, the field position and size are also stored in the form of lines and pixels per line in the segment buffer 7, the data respectively stored last not being overwritten. The storage capacity of the segment buffer 7 is thus about double said data to be stored

for a field, which in each case corresponds to a field in an instantaneous segment and a current segment in the memory 2.

Each time the write pointer is incremented, the write controller 4 additionally checks whether the new address has a specific offset, with respect to the previously stored (not with respect to the currently stored) address. This offset may also be zero in the case of a high vertical decimation factor. It serves essentially as a safety margin in order to avoid overtaking as a result of asynchronous data acceptance or slightly deviating vertical frequencies. With this offset, an overtake signal is generated which indicates whether the address has been reached again and hence this picture content has been overwritten.

The content of the segment buffer 7 is transferred to the read controller 5, by means of which the memory 2 is read beginning at one of the two addresses present after the start of reading at the insertion position, so that the inset picture can be generated in accordance with its position and size in the main picture by the insertion apparatus 3.

On the basis of the overtake signal transmitted by the write controller 4, the display controller 6 decides which of the two segments present in the memory 2 is read out. The selection of the segment initially always proceeds from the last segment. If overtaking took place before the start of reading, then the instantaneous (current) segment is read out. A corresponding segment selection signal is transmitted to the read controller 5.

The insertion position is also calculated by means of the display controller. The display controller 6 furthermore serves for correcting the raster positions, this being effected by comparison between the raster

position of a displayed picture and the raster position of a stored picture and skipping or repetition of a line. Finally, the display controller 6 can also be utilized for multi-picture insertion.

Before the algorithm is described in detail, firstly the terms used in this context will be explained.

As was explained above, the decimated pixels of the inset picture are firstly stored in the memory 2. For display purposes, they are read from the memory again in the temporal framework of the main picture. For this purpose, the write and read addresses have to be generated by separate address counters.

Figure 2 shows the corresponding signal profiles when writing to the memory 2. The instantaneous value of the write address counter represents a write pointer with a decimated inset pixel in the memory 2. The terms "write pointer" and "read pointer" shall be used for this reason.

An acquisition window (vaqwin) begins with a pulse (vaqstart), and the write address pointer rises with each decimated pixel. Since only the visible part of the inset picture is decimated, the write address pointer rests whenever there is no valid line available from the vertical decimation stage. After the last line to be decimated, the pointer is reset to the start position. The picture of a ramp with shoulders results in the representation.

Figure 3 shows the corresponding signal profiles when reading from the memory 2. The instant at which a start signal (vdisstart) must be generated in order to begin reading from the memory 2 is calculated by means of the display controller 6 on the basis of the desired insertion position of the decimated inset picture in the main picture. With each line of the main picture,

at the corresponding insertion position (hdisstart), a line of the decimated inset picture is then read from the memory and inserted into the main picture (video mux).

The picture of a ramp with shoulders once again results in the representation of the read address pointer. The ramps of the read and write address pointers differ in respect of their average gradient. The latter will be considered in detail below since it represents the rate at which a number of memory cells are swept over within a specific period of time.

The speed of the write address pointer changes with the decimation factor, to be precise in such a way that the ramp of the write address pointer becomes less steep as the decimation factor rises.

Figure 4 shows the origination of a seam for the case of representation in the frame mode. If only a field memory is present and the inset picture has been decimated, the write pointer is generally overtaken by the read pointer. Since the sources for the inset picture ("insert_field") and the main picture ("parent_field") are generally asynchronous with respect to one another, a seam is thus produced. In Figure 4, this is indicated by the point of intersection between the relatively slow write pointer and the read pointer that overtakes the latter, the upper-case letters A, B designating the raster position of the inset picture and the lower-case Greek letters α, β designating the raster position of the main picture.

From a temporal standpoint, the current field is read before the seam, while part of an older picture is reproduced after the seam. It should be noted in this case that, as a result of the line interlacing method (interlaced mode), the raster position changes in the

event of overtaking, and this subsequently has to be corrected again.

The seam becomes very clearly visible in particular when a moving picture is displayed, that is to say when the current picture and the older picture contain different motion phases. If different standards are used for the main picture and the inset picture, then rolling of the seam occurs. As a result of different frame frequencies, the combination of the raster positions at the beginning of the representation changes a number of times every second. It is a very complicated procedure to perform a correction in a manner dependent on this incorrect position. Moreover, the picture can be very erratic in the vertical direction and be perceived as unpleasant.

The method according to the invention and the circuit arrangement according to the invention now allow, in particular in the frame mode, a seamless representation of pictures that have been decimated to different extents, without two separate field memories having to be available.

For the explanations below, it will be assumed that orthogonal memory division has been chosen. As a result, the memory is divided into lines with fixed start addresses. The length of such a line in the memory is determined by the largest picture.

Furthermore, it will be assumed that the inset picture and the main picture are present in the same standard. The two picture sources can be asynchronous but, in terms of their time frame, should initially have no deviations from one another. If the inset picture is not decimated vertically and horizontally, one field memory suffices for generating a seamless picture-in-picture representation, since the two address pointers cannot overtake one another on account of their

identical speed. The case of raster position correction forms an exception. This correction is performed in the first line given a corresponding combination of main and inset picture positions.

In this case, the read address pointer jumps by one line. In the course of this jump, the situation where the write address pointer is overtaken must be prevented. This is achieved in that there is space for two additional lines in the memory.

Furthermore, suitable control of the memory accesses is necessary. The memory is written to with the fields in a circulating manner. As a result, with each new field, the start address is shifted by the number of additionally present lines in the direction of lower physical addresses. If the physical end address of the memory is reached in the course of writing, then a jump is made back to the start address.

Figure 5 shows the corresponding signal profiles during write control (a) and read control (b). Accordingly, there is thus always somewhat more than one inset field in the memory. In a similar manner to the case of the organization of two field memories, in this case, too, the write address pointer determines the memory segment enable. The signals "vaqstart", "vaqwin", "vdisstart" and "hdisstart" again have the same meaning as in Figures 2 and 3.

Figure 6 shows a block diagram for selecting the respectively valid memory segment. The circuit comprises an address counter 12, whose output is connected to a first register 10 and to a first input of a comparator 14, a second register 11, to whose input the output of the first register 10 is connected, and also a multiplexer 13, whose first input (line_adr_next) is connected to the output of the first register 10 and whose second output is connected to the

output of the second register 11. This latter output is also connected to a second input of the comparator 14, whose output is connected to a flip-flop 15.

For control of the read accesses, the start addresses of the old and new inset fields are stored in the registers 10, 11. With the beginning of a new field, the older of the two register contents is rejected, and the formerly new start address becomes the old address, while the present current address becomes the new start address. If the beginning of the older inset field has been overwritten as a result of the memory being written to in a circulating manner, it can no longer be read.

For selection of the valid memory segment, the content of the address counter 12 (line_address) is continually compared with the start address of the older of the two fields (line_address_cur) in the comparator 14. In the event of correspondence, the flip-flop 15 is set and the start address of the new field is then present at the output of the multiplexer 13. If a new field is begun, then the flip-flop is reset, and, as a result of the change of the register contents, the same start address as before is present at the output of the multiplexer 13, until this is also overwritten again. In this way, the memory enable points to a valid memory segment at every instant. The memory space that is additionally present means that the read pointer cannot reach or overtake the write pointer even in the event of a jump on account of the raster position correction.

In order to satisfy the general requirements, however, this sequence must be extended. Considerable deviations from the standard can occur particularly in the case of video recorders which are operated with fast forward or rewind with picture reproduction. In this case, by way of example, it is also necessary to take account of the maintenance state and the wear of the tape material.

The memory control must be able to compensate for the effects of a stretched tape and also synchronism fluctuations of the drive mechanism. However, a precondition in this case is that the sync pulse separation still operates correctly in the case of such a signal.

The vertical frequency f_V and the horizontal frequency f_H are related through the number Z of lines as follows:

$$f_V = f_H / Z \qquad (5.1)$$

The line frequencies of the main picture (f_{Hp}) and of the inset picture (f_{Hi}) are of interest for the algorithm. Their fluctuations directly affect the writing and reading speed. The larger the line frequency f_{Hi} of the inset picture, the more memory content is written per unit time. The smaller the line frequency f_{Hp} of the main picture, the fewer lines are read per unit time. The opposite correspondingly holds true.

If the same standard is used in both sources, then the following relationships hold true, where f_H is the desired line frequency:

$$f_{Hi\_max} = f_H (1 + df_{Hi}) \qquad (5.2)$$

$$f_{Hi\_min} = f_H (1 + df_{Hi}) \qquad (5.3)$$

$$f_{Hp\_max} = f_H (1 + df_{Hp}) \qquad (5.4)$$

$$f_{Hp\_min} = f_H (1 + df_{Hp}) \qquad (5.5)$$

It will additionally be assumed that no vertical picture decimation is performed. Since the sources are again two sources that are asynchronous with respect to one another, write and read pointers can adopt any desired position with respect to one another. Equally, the pointers can overtake one another in both

directions given corresponding combination of the horizontal frequencies.

Figure 7 shows the memory lines required for the respective write and read pointers, where Z_{acq} is the number of picture lines of a field that are used for acquisition. The representation makes it clear how many lines must additionally be present in the memory in order to prevent overtaking of the pointers in both directions.

$$Z_{s2} = Z_{acq} \{ (f_{Hi\_max} - f_{Hp\_min}) / f_{Hi\_max} \} \quad (5.6)$$

$$Z_{s1} = Z_{acq} \{ (f_{Hp\_max} - f_{Hi\_min}) / f_{Hp\_max} \} \quad (5.7)$$

The total amount of additionally required memory for the seamless picture-in-picture representation turns out to be:

$$Z_g = Z_{acq} + Z_{s1} + Z_{s2} \quad (5.8)$$

During writing, the memory contains part of an old field and part of a new field. Through the position of the write address pointer, one of the two fields is enabled for reading. If fewer than Z_{s1} lines of the new field have been written, the old field is enabled. Otherwise, the distance from the beginning of the old field is less than Z_{s2} lines, with the result that the new field can be read.

Figure 8 shows the memory division in the case where no vertical decimation is performed.

If decimation is then effected in the horizontal and vertical direction, this influences the speed of the write address pointer. The corresponding relationships are shown in Figure 9. The rise of the ramp is smaller in this figure.

It will initially be assumed that the writing speed changes to a considerable extent as a result of the decimation. By contrast, the fluctuations due to changes in the line frequency shall be small.

It follows from this that the read pointer can no longer be overtaken by the write pointer on account of the speed difference. As a result, the memory outlay for seamless picture-in-picture representation can now be determined using the decimation factors and the fluctuation range of the picture sources.

$$Z_{s1\_dec}(dec_{ver}) = (Z_{acq}/dec_{ver})(1-f_{Hi\_min}dec_{ver}/f_{Hp\_max}) \qquad (5.9)$$

The additional requirement of lines decreases as the decimation factor increases. The maximum emerges for a vertical decimation factor dec_{ver} of 1 (vertically undecimated picture).

The possibility of the read pointer being overtaken by the write pointer will now also be taken into account. For small vertical decimation factors, the result is a further additional memory requirement of:

$$Z_{s2\_dec} = (Z_{acq}/dec_{ver})\ (1-f_{Hp\_min}\ dec_{ver}/f_{Hi\_max}) \qquad (5.10)$$

For a meaningful result, the expression in the right-hand brackets must be positive. The validity of this expression is thus limited to a range of:

"1" less than equal to "dec_{ver}" less than equal to "(f_{Hi_max}/f_{Hp_min})" (5.11)

For values which are greater than the right-hand limit, Z_{s2_dec} shall be set to zero.

Taking account of the validity ranges, the additional memory requirement results from the sum of Z_{s1_dec} and

Z_{s2_dec}. The examinations made at the beginning are a special case for a vertical decimation factor of 1.

The total memory requirement consequently turns out to be:

$Z_g(dec_{ver}) = Z_{acq}/dec_{ver} + Z_{s1\_dec} + Z_{s2\_dec}$ for "1" less than equal to "dec_{ver}" less than equal to "f_{Hi_max}/f_{Hp_min})" (5.12)

thus resulting in the following:

$Z_g(dec_{ver}) = Z_{acq}/dec_{ver}(3 - f_{Hp\_min}\ dec_{ver}/f_{Hi\_max} - f_{Hi\_min}/(dec_{ver}\ f_{Hp\_max})$ (5.14)

Otherwise, the following holds true:

$Z_g(dec_{ver}) = Z_{acq}/dec_{ver} + Z_{s1\_dec}$ for "dec_{ver}" greater than "(f_{Hi_max}/f_{Hp_min})" (5.13)

The following results from this:

$Z_g(dec_{ver}) = Z_{acq}/dec_{ver}\ (2 - f_{Hi\_min}/(dec_{ver}\ f_{Hp\_max})$ (5.15)

The total number of memory cells required has its maximum for a vertical decimation factor of 1. As the decimation factor increases, the memory cell requirement greatly decreases.

It shall also supplementarily be pointed out that when the memory 2 is extended to three segments, the method according to the invention can also be employed with a frame frequency of 100 Hz in the AABB raster.

Patent claims

1. A method for picture-in-picture insertion,
in which a sequence of decimated inset pictures is written to a memory device (2) and is read out for insertion into a sequence of main pictures,
characterized
in that the inset pictures are written to the memory device (2) in a circulating manner as fields under continuously incremented write addresses, the inset pictures being written to corresponding memory segments beginning at corresponding writing start addresses,
in that the writing start address of each written-in field is stored,
in that, each time the write address is incremented, by comparison of the respective instantaneous write address with a previously stored writing start address, an overtake signal is formed which indicates whether the respective writing start address is reached again and the memory segment corresponding to the respective writing start address is overwritten,
in that, by evaluation of the overtake signal, the memory segment corresponding to the last writing start address stored or the penultimate writing start address stored is selected for read-out, and
in that the selected memory segment is read out for insertion into the respective main picture with continuously incremented read addresses.

2. The method as claimed in claim 1,
characterized in that the write and read addresses are continuously incremented from a first memory address up to a last memory address and are in each case reset to the first memory address again after the last memory address has been reached.

3. The method as claimed in claim 1 or 2, characterized in that, in order to insert an inset picture into a main picture, in a segment buffer (7) for two inset pictures, the picture position and size are in each case stored in the form of a number of lines and also pixels per line.

4. The method as claimed in one of the preceding claims, characterized in that raster correction is effected by comparison between the raster position of a picture to be displayed and the raster position of a stored picture and also by skipping or repeating a line.

5. The method as claimed in one of the preceding claims, characterized in that, each time the write address is incremented, the instantaneous write address is compared with the penultimate writing start address stored and, in the event of correspondence, the last writing start address stored is used as reading start address for reading the corresponding memory segment, whereas otherwise the penultimate writing start address is used as reading start address for reading the corresponding memory segment.

6. A circuit arrangement for inserting a sequence of decimated inset pictures into a sequence of main pictures, having a write controller (4) for writing the inset pictures as fields under continuously incremented write addresses to corresponding memory segments of a memory device (2) beginning at corresponding writing start addresses,

having a segment buffer (7) for storing the writing start address of each field written to the memory device (2), in which case an overtake signal can be generated by the write controller (4) each time the write address is incremented, by comparing the respective instantaneous write address with a previously stored writing start address, which overtake signal indicates whether the respective writing start address is reached again and the memory segment of the memory device (2) which corresponds to the respective writing start address is overwritten,

having a display controller (6) to which the overtake signal is fed, in which case the display controller (6) can select, by evaluating the overtake signal, the memory segment corresponding to the last writing start address stored or the penultimate writing start address stored, for read-out by a read controller (5) - connected to the segment buffer (7) - with the aid of continuously incremented read addresses and for insertion into the respective main picture.

7. The circuit arrangement as claimed in claim 6, characterized in that the write controller (4) and the read controller (5) each have an address counter (12) for incrementing the write addresses and read addresses, respectively.

8. The circuit arrangement as claimed in claim 6 or 7, characterized in that, by means of the display controller (6), an insertion position of an inset picture is calculated and a corresponding insertion signal can be fed to an insertion apparatus (3).

9. The circuit arrangement as claimed in one of claims 6 to 8,

characterized in that, by means of the display controller (6), raster correction can be carried out by comparison between the raster position of a picture to be displayed and the raster position of a stored picture and also by skipping or repeating a line.

10. The circuit arrangement as claimed in one of claims 6-9,
characterized
in that provision is made of a comparator (14) for comparing the instantaneous write address provided by an address counter (12) with the penultimate writing start address stored, the output of the comparator (14) being connected to a flip-slop (15) for driving a multiplexer (13), and
in that the penultimate writing start address stored is present at a first input of the multiplexer (13) and the last writing start address stored is present at a second input of the multiplexer (13), with the result that, in the event of correspondence between the instantaneous write address of the address counter (12) and the penultimate writing start address stored, the multiplexer (13) outputs the last writing start address stored as reading start address, whereas otherwise the multiplexer (13) outputs the penultimate writing start address stored as reading start address.

GR 99 P 1352

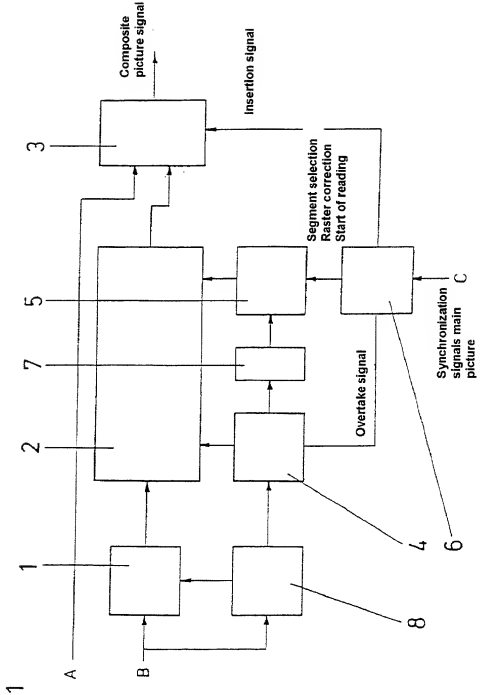


FIG1

FIG 2

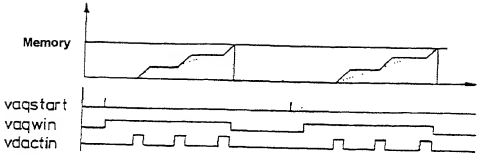


FIG 3

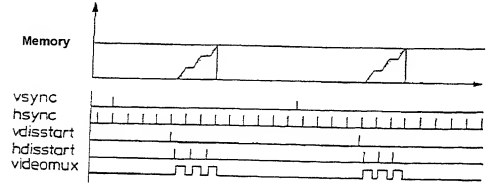


FIG 4

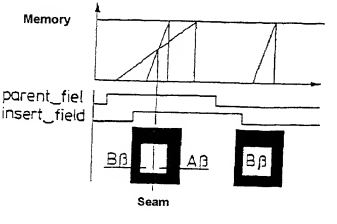


FIG 5a

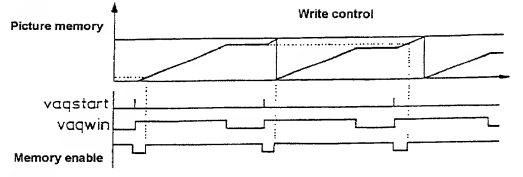


FIG 5b

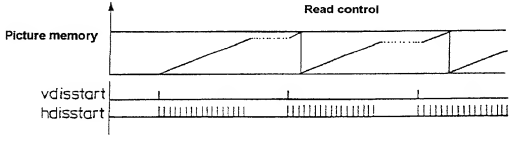


FIG 6

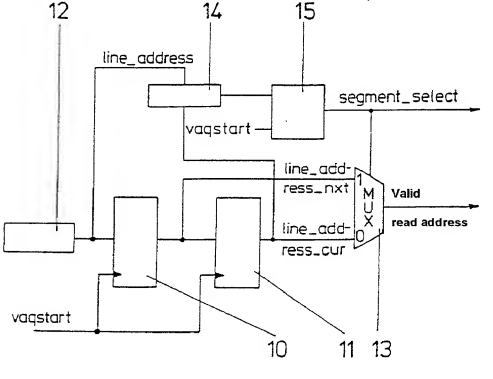


FIG 7

FIG 8

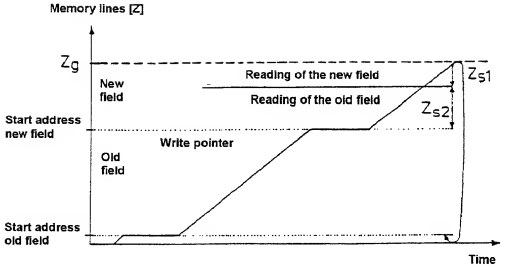
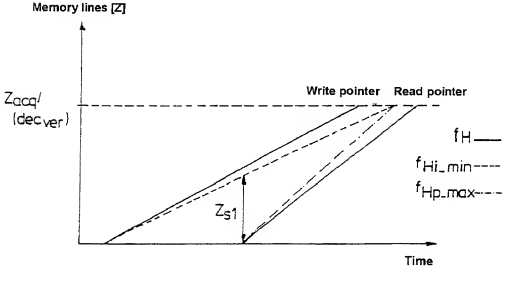

Memory lines [Z]
Zg
New field
Reading of the new field
Reading of the old field
Zs1
Zs2
Start address new field
Write pointer
Old field
Start address old field
Time

FIG 9


Memory lines [Z]
Zacq/ (decver)
Write pointer
Read pointer
fH
fHi_min
fHp_max
Zs1
Time

Docket No. 56426
Page 1 of 3

Declaration and Power of Attorney for Patent Application
English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND CIRCUIT ARRANGEMENT FOR PICTURE-IN-PICTURE INSERTION

the specification of which

(check one)

[X] corresponds to and claims priority of PCT/DE00/00681, filed March 3, 2000 which application claims priority of German Patent Application No.: DE 199 09 562.0, filed March 4, 1999.

[ ] was filed on _____ as United States Application No. or PCT Application No. _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
DE 199 09 562.0 (Number)	Germany (Country)	04 March 1999 (Day/Month/Year Filed)	[ ]
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	[ ]
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	[ ]

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. Section 120 of the United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark office all information known to me to be material to patentability as defined in Title 37, C.F.C., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
PCT/DE00/00681	3 March 2000	Pending
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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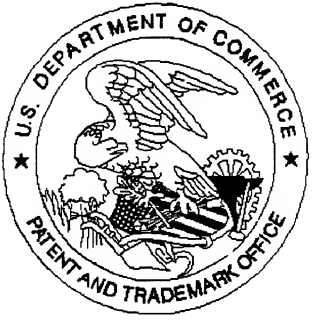

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☒ ***Scanned copy is best available.*** Drawing figure 7 is oblique.